



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,024	09/18/2003	Reid Hayhow	10030557-1	7952
63448	7590	01/31/2008		
VERIGY 4700 INNOVATION WAY, BLDG D1 FORT COLLINS, CO 80528			EXAMINER CHUNG, PHUNG M	
			ART UNIT 2117	PAPER NUMBER
			MAIL DATE 01/31/2008	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/666,024	Applicant(s) HAYHOW, REID	
	Examiner Phung My Chung	Art Unit 2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 October 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. In view of the Appeal Brief filed on 10/26/07, PROSECUTION IS HEREBY REOPENED. The New ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

Supervisory Patent Examiner
Technology 2100

Jacques Louis-Jacques
JACQUES LOUIS-JACQUES
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action: (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hughes, Jr. (4,493,079) in view of Regelman et al (6,574,626).

As per claim 1, Hughes, Jr. discloses a method comprising:

reading a test file including a plurality of test vectors to be applied to a device.

(See col. 3, lines 51-61). Hughes, Jr. does not disclose determining a required memory needed to execute the plurality of test vectors. However, Regelman et al disclose

determining a required memory needed to execute the plurality of test vectors.

(See col. 2, lines 21-24, lines 31-34, lines 60-67 to col. 3, lines 1-5). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the step of determining a required memory needed to execute the plurality of test vector as taught by Regelman et al into the invention of Hughes, Jr. so that it permits efficient and cost effective use of memory to achieve optimal program storages and performance (col. 4, lines 13-19).

As per claim 2, Regelman et al further disclose wherein determining a required memory comprises determining a required memory needed for each of a plurality of boards (integrated circuit wafer) of a tester to execute the test vectors for the board.

As per claim 3, Regelman et al further disclose wherein determining a required memory comprises determining a required memory needed for each of a plurality of pins (test points/channels) of a tester to execute the test vectors for the pin (col. 4, lines 5-20).

As per claim 4, Regelman et al further disclose wherein determining a required memory comprises counting the number of test vectors for each test in the test file (col. 2, lines 21-24 and col. 4, lines 42-43).

As per claim 5, Regelman et al further disclose wherein determining a required memory comprises: determining a first memory requirement needed for a first pin of a tester to execute the test vectors for a first test in the test file; setting the required memory equal to the first memory requirement; and for each additional pin of the tester, determining a second memory requirement needed for the additional pin to execute the test vectors for the first test; and if the second memory requirement is greater than the first memory requirement, setting the required memory equal to the second memory requirement. (See col. 20, lines 50-54).

As per claim 6, Both Hughes, Jr., col. 5, lines 16-28 and Regelman et al, col, 20, lines 50-54, disclose for each additional test in the test file:

for each pin of the tester, determining a third memory requirement for the pin to execute the test vectors for the additional test; and setting the required memory equal to

the third memory requirement if the third memory requirement is greater than the required memory.

As per claim 7, Regelman et al further disclose if the required memory exceeds an existing memory allotment, increasing the allotment of memory (col. 2, lines 31-34. and col. 20, lines 50-54).

As per claims 8-9, the teaching of Hughes and Regelman et al do not disclose if the required memory exceeds an existing memory allotment, notifying a user of an amount of additional memory required. However, Regelman et al disclose checking if the required memory exceeds an existing memory allotment (col. 13, lines 17-23, col. 16, lines 8-10) and Regelman et al also disclose if additional software units are required, the memory management process communicates to the user that one or more necessary software are not available. The user then determines which new test file is required (col. 20, lines 1-4). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to set the memory management process to notify the user of an amount of additional memory required if the required memory exceeds an existing memory allotment so that the user can provides sufficient memory space as test pattern increase in size in order to accommodate the entire test program.

As per claim 10, this claim is rejected under similar rationale as set forth in claim

1.

As per claim 11, this claim is rejected under similar rationale as set forth in claim

2.

As per claim 12, this claim is rejected under similar rationale as set forth in claim 3.

As per claim 13, this claim is rejected under similar rationale as set forth in claim 4.

As per claims 14-15, these claims are rejected under similar rationale as set forth in claims 8-9.

As per claim 15, this claim is rejected under similar rationale as set forth in claim 9.

As per claim 16, Hughes and Regelman et al do not specifically disclose using the required memory to bill a customer. However, Regelman et al disclose determining a required memory needed to execute the plurality of test vectors (col. 2, lines 21-24, lines 31-34, lines 60-67 to col. 3, lines 1-5). Therefore, it would have been obvious to a person of skilled in the art, at the time the invention was made, based on the determining of the required memory needed to execute the plurality of test vectors, to bill a customer using the required memory when desired if needed.

Response to Arguments

4. Applicant's arguments filed on 10/26/07 have been fully considered but they are not persuasive because:

Firstly, applicant argues that, claims 1, 7-10 and 14-15, Regelman does not teach the step of determining a required memory needed to execute the plurality of test vectors.

Examiner disagrees with applicant because Regelman does teach the step of determining a required memory needed to execute the plurality of test vectors. (See col. 2, lines 21-24, lines 31-34, lines 60-67 to col. 3, lines 1-5). Therefore, claims 1, 7-10 and 14-15 are still remain rejected.

Secondly, applicant argues that, claims 2-4 and 11-13, Regelman does not teach determining a required memory needed for each of a plurality of boards of a tester to execute the test vectors for the board; determining a required memory needed for each of a plurality of pins of a tester to execute the test vectors for the pin; and counting the number of test vectors for each test in the test file.

Examiner disagrees with applicant because Regelman does teach these steps:

As per claim 2, Regelman et al further disclose wherein determining a required memory comprises determining a required memory needed for each of a plurality of boards (integrated circuit wafer) of a tester to execute the test vectors for the board.

As per claim 3, Regelman et al further disclose wherein determining a required memory comprises determining a required memory needed for each of a plurality of pins (test points/channels) of a tester to execute the test vectors for the pin (col. 4, lines 5-20).

As per claim 4, Regelman et al further disclose wherein determining a required memory comprises counting the number of test vectors for each test in the test file (col. 2, lines 21-24 and col. 4, lines 42-43).

As per claims 11-13, these claims are rejected under similar rationale as set forth in claims 2-4.

Thirdly, applicant argues that, claims 5-6, Regelman does not teach determining a required memory comprises: determining a first memory requirement needed for a first pin of a tester to execute the test vectors for a first test in the test file; setting the required memory equal to the first memory requirement; and for each additional pin of the tester, determining a second memory requirement needed for the additional pin to execute the test vectors for the first test; and if the second memory requirement is greater than the first memory requirement, setting the required memory equal to the second memory requirement.

Examiner disagrees with applicant because Regelman (col. 20, lines 50-54), does disclose determining a required memory comprises: determining a first memory requirement needed for a first pin of a tester to execute the test vectors for a first test in the test file; setting the required memory equal to the first memory requirement; and for each additional pin of the tester, determining a second memory requirement needed for the additional pin to execute the test vectors for the first test; and if the second memory requirement is greater than the first memory requirement, setting the required memory equal to the second memory requirement. Therefore, claims 5-6 are remain rejected.

Fourthly, applicant argues that, claim 16, Regelman does not teach a customer should be billed based on a required memory needed to execute a plurality of test vectors.

Examiner disagrees with applicant because Hughes and Regelman et al do not specifically disclose using the required memory to bill a customer. However, Regelman et al disclose determining a required memory needed to execute the plurality of test

vectors (col. 2, lines 21-24, lines 31-34, lines 60-67 to col. 3, lines 1-5). Therefore, it would have been obvious to a person of skilled in the art, at the time the invention was made, based on the determining of the required memory needed to execute the plurality of test vectors, to bill a customer using the required memory when desired if needed.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phung My Chung whose telephone number is 571-272-3818. The examiner can normally be reached on Monday to Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on 571-272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Phung My Chung
Primary Patent Examiner